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The main overall goal of this project was to improve the high speed performance of transistors and integrated circuits based on silicon, which is the material on which most microelectronic circuitry (such as microprocessors and memory chips) is based. This project examines the scaling of MOSFET's to very small channel dimensions using a vertical structure which is defined by Rapid Thermal Chemical Vapor Deposition. The scaling of vertical p-channel MOSFET's with the source and drain doped with boron during low temperature epitaxy is limited by the diffusion of boron during subsequent side wall gate oxidation. By introducing thin SiGeC layers in the source and drain regions, this diffusion has been suppressed, enabling for the first time the scaling of vertical p-channel MOSFET's to under 100nm in channel length to be realized. Device operation with a channel length down to 25nm has been achieved.

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FINAL TECHNICAL REPORT

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Abstract

The main overall goal of this project was to improve the high speed performance of transistors and integrated circuits based on silicon, which is the material on which most microelectronic circuitry (such as microprocessors and memory chips) is based. This project examines the scaling of MOSFET's to very small channel dimensions using a vertical structure which is defined by Rapid Thermal Chemical Vapor Deposition. The scaling of vertical p-channel MOSFET's with the source and drain doped with boron during low temperature epitaxy is limited by the diffusion of boron during subsequent side wall gate oxidation. By introducing thin SiGeC layers in the source and drain regions, this diffusion has been suppressed, enabling for the first time the scaling of vertical p-channel MOSFET's to under 100nm in channel length to be realized. Device operation with a channel length down to 25nm has been achieved.

Introduction to Technical Approach:

Vertical MOSFET's are attractive structures for short channel MOSFET's because the channel length (L) may be determined by the thickness of an epitaxial layer instead of by lithography resolution. The chip area can also be reduced in some cases by using vertical structures [1,2]. Furthermore by using ultra-thin pillars (width<100nm), the channel region can be fully-depleted by surrounding gates, resulting in improved subthreshold slope and suppression of short channel effects [3,4]. Sub-100nm n-channel vertical MOSFET's have already been reported [5,6]. However the shortest previous results for vertical p-channel MOSFET's have L of 0.25μm [7] for a uniform pillar structure and 0.13μm for edges of selective epitaxy facets [8]. The main problem is the source/drain dopant (boron) diffusion during gate oxidation after epitaxy and pillar-formation, or during annealing after source and drain dopant implantation. This diffusion is dramatically enhanced by gate oxidation. In this work, we solve this diffusion problem by the use of SiGeC which is shown to be useful in eliminating the oxidation-enhanced diffusion. We then introduced novel SiGeC layers in source and drain of vertical transistors to stop boron diffusion and hence successfully scaled the channel length down to 25nm for the vertical p-channel MOSFET's.

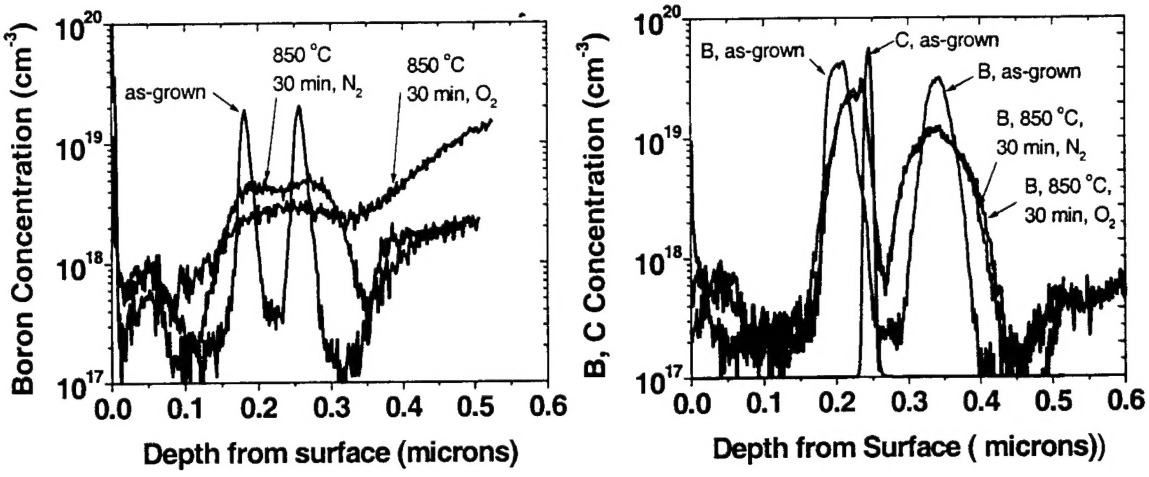
Results and Impact/Applications:

Fundamental Interaction of Carbon on Boron Diffusion through Silicon Interstitials

i-Si, 1500Å, 700°C
Si : boron $3x10^{19}/cm^3$, 250Å, 700°C
i-Si, 100Å, 700°C
i-$Si_{1-x-y}Ge_xC_y$, 250Å, 625°C
i-Si, 400Å, 700°C
Si : boron $3x10^{19}/cm^3$, 250Å, 700°C
i-Si, 1500Å, 700°C
Si buffer layer : boron $3x10^{19}/cm^3$, 2500Å, 1000°C

Fig.1. Test structure to study boron oxidation enhanced diffusion and transient enhanced diffusion. Two boron markers are separated by a $Si_{1-x-y}Ge_xC_y$ interstitial sink layer (x = [0 - 0.2]; y = [0 - 0.005]) (Ref. 10)

As described above, OED can increase diffusion by an order of magnitude or more at low process temperatures. It is mediated by interstial silicon atoms. SiGeC has previously been shown to be capable of reducing transient enhanced diffusion (TED) of boron caused by ion implantation [9], which is also mediated by intersititials. We then used the structure of Fig. 1 to probe the use of SiGeC to reduce OED. The structure has two marker layers of highly-boron-doped silicon layers designed to measure the reduction of oxidation enhanced diffusion of boron (OED) [10]. OED is caused by the injection of interstitial Si atoms, which are necessary for the diffusion of boron. One boron layer is above and one is below a $Si_{1-x-y}Ge_xC_y$ region designed to capture interstitials, which are introduced from the surface during oxidation. While the exact mechanism is not well understood, it appears that substitutional C creates a sink for Si interstitials, which are required for the diffusion of dopant atoms such as boron. By reducing the local interstitial concentration, diffusion coefficients can thus be reduced, not just in the SiGeC region but also in nearby silicon regions. Note in Fig.2 that in the control sample without any SiGeC (Fig 2(a.)) there is a substantial increase in the diffusion coefficient when the samples are annealed in oxygen as opposed to in nitrogen. Modelling the SIMS curves show an increase of the diffusion coefficient by nearly an order of magnitude. In the sample of Fig. 2(b.), a $Si_{0.8}Ge_{0.2}C_{0.005}$ layer was inserted between the boron marker layers. In this sample no OED was observed for the lower boron peak, showing that all of the injected interstitials were effectively captured [10].



(a) (b.)

Figure 2. SIMS of boron and carbon levels (C as-grown only) in buried marker layers as-grown and after annealing at 850 °C in either N_2 or O_2 in (a.) control sample with no SiGeC and (b.) sample with SiGeC layer between the two boron layers. Note the elimination of OED in the lower boron-doped layer in sample (b.) [10].

Vertical p-channel MOSFET's

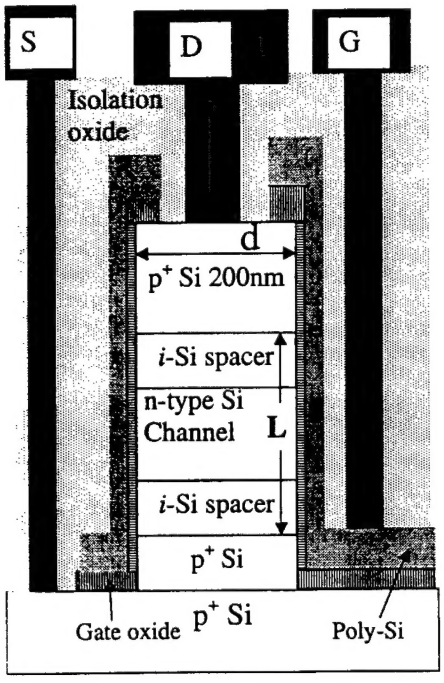


Fig. 3. Cross-section of vertical p-channel MOSFET's with Si only (no SiGeC layers).

The cross-section of our initial vertical p-channel MOSFET's without any SiGeC layers is shown in Fig. 3. The p^+np^+ epitaxial layers were grown by rapid thermal chemical vapor deposition on a Si (100) p-type substrate[11]. 26 sccm Dichlorosilane was used as Si source. The system pressure was maintained at 6 torr with a hydrogen flow of 3 slpm. Epitaxial layers were doped *in situ* using B_2H_6 and PH_3. Following a p^+ buffer layer grown at 1000°C with a boron doping of $6x10^{19}cm^{-3}$, an n-type Si channel (doping $1\sim5x10^{18}cm^{-3}$) was grown at 700°C with undoped spacer layers on each side of the channel. In this work we used wide rather than ultra-thin pillars, so the channel was doped in order to suppress punch-through. Special steps were necessary to achieve a sharp phosporous profile in the channel and will be discussed elsewhere. The channel length is defined as the epitaxial layer thickness between the two p^+ layers, with the edge of the p^+ profile defined as the point when the boron concentration (as

measured by secondary ion mass spectroscopy (SIMS)) drops to $1/\sqrt{2}$ of its value in the heavily doped source/drain, multiplied by 1.1 to account for the fact that the side walls were not perfectly vertical. Fig. 4 gives SIMS profiles of boron in the as-grown p^+np^+ structures, which demonstrate the abrupt profiles before any further high temperature processes. The boron slopes are 8nm/dec and 12nm/dec on upper and lower edges respectively, and are limited by SIMS resolution. (The worse profile on lower interfaces is caused by the primary Cs^+ beam knocking in B atoms further into the substrate). Vertical islands were created by optical lithography and reactive ion etching. The island edges were aligned with the [011] and [01$\bar{1}$] crystal direction on the substrate. The slope of the walls was ~25° off from perfectly vertical.

Sacrificial and gate oxidations were performed at 750°C in wet O_2 to give either a 6nm or 10nm sacrificial oxide followed by a 6 or 10nm gate oxide. These oxide thickness and all others reported in our work were all measured on a planar (100) crystal Si control wafer oxidized simultaneously with the FET's. Higher oxide thickness are expected on the side walls, which have a nominal (110)-like surface orientation. (An oxidation rate enhancement of 60~80% has been reported on a (110) vs. a (100) surface at 800°C in dry O2 for oxide thickness in the 6~10nm range on (100) surfaces[10]). Because the Si islands in this work are large (~50 x 50μm^2), 2-D effects on the side walls (vs. those in small pillars) can probably be neglected. 200nm p^+-polysilicon gates were deposited at 700°C with in-situ doping of $2x10^{21}cm^{-3}$ (from SIMS) giving a sheet resistance of 10Ω/!. No gate depletion effects were observed in planar MOS capacitors using the same gates as a result of the high active doping concentration levels in the gates. The final process steps were poly-Si dry-etching and back-end processing.

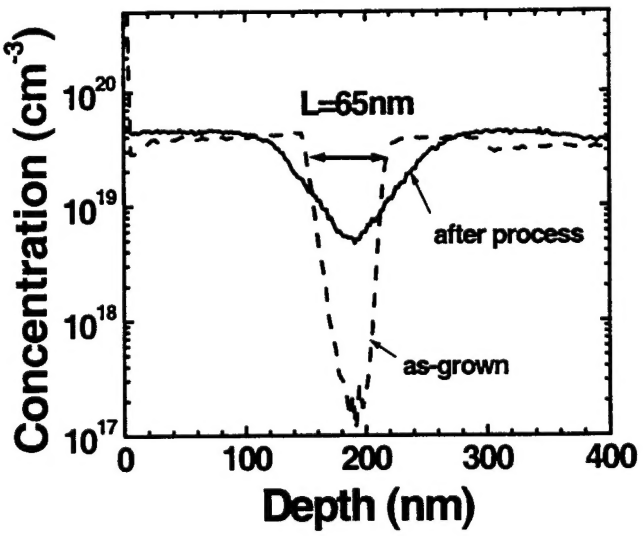
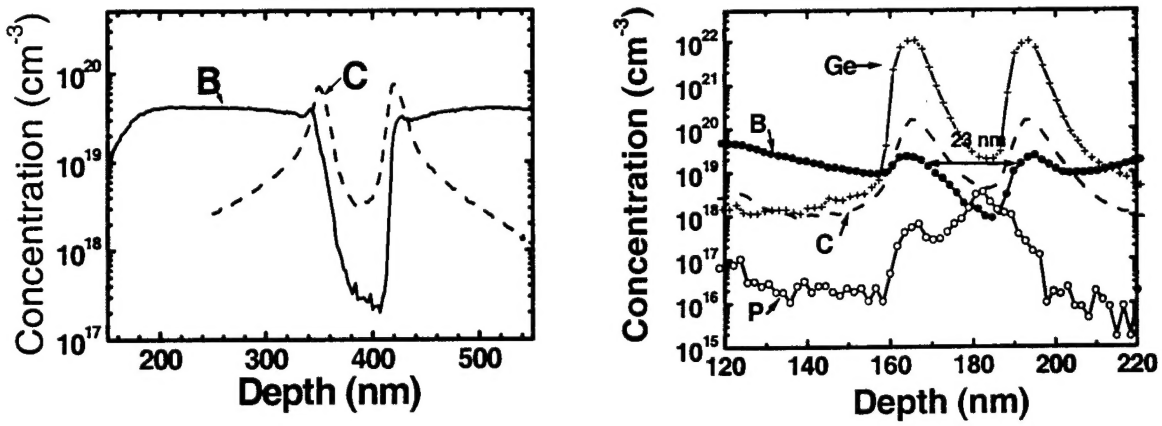


Figure 4. SIMS profiles from as-grown samples (dashed line) and after wet oxidation at 750°C and 700°C poly-Si deposition (solid line) for structures with Si only (no SiGeC).

Fig. 4 also gives the SIMS result from the same sample after all the high temperature processing. It shows that boron in the source and drain has diffused into channel, which limits the channel length in practice to »100nm. Note in the literature vertical p-channel MOSFET's by a similar process were limited to L>130nm[7,8], although a high pressure (10bar) wet oxidation at low temperature (600°C) was required to limit diffusion[8,13]. For our process, devices with L=0.5μm are well behaved, but those with L=0.1μm (as grown) are shorted. Simulations showed most of this diffusion to be caused by the well known oxidation enhanced diffusion (OED) effect, in which injected interstitials greatly increase the diffusion of boron [9].

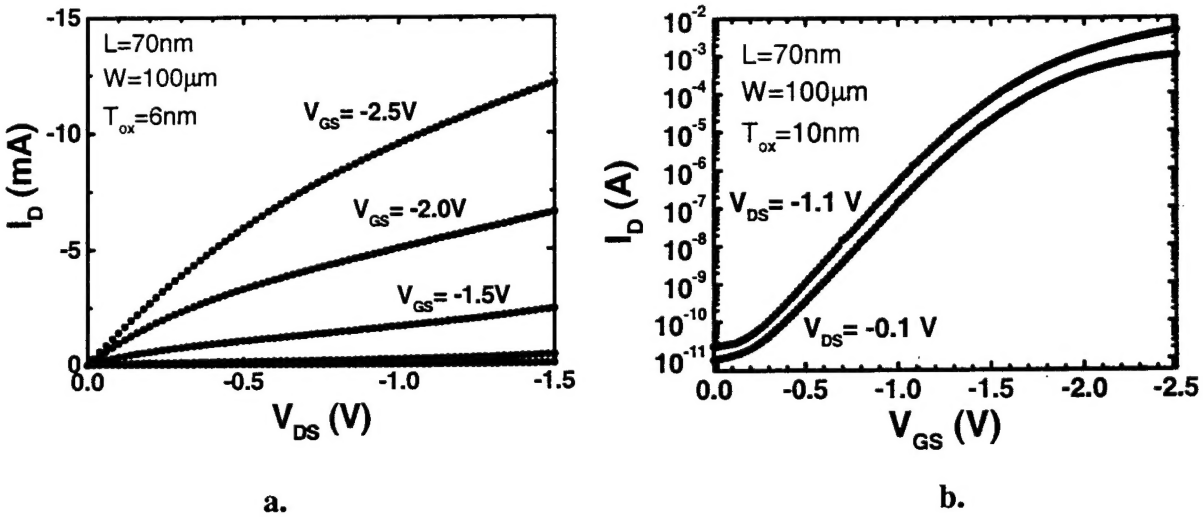


(a) (b)

Figure 5. (a) SIMS profiles for vertical p-channel MOSFET's with 20nm undoped $Si_{0.976}Ge_{0.2}C_{0.004}$ epitaxial layers after the same high temperature process conditions as in Fig 2. The mesa structure is shown in the inset. (b) SIMS profiles for a L=25nm device sample with highly B-doped SiGeC layers after all the high temperature processing.

The work in the previous section work has shown that SiGeC can getter interstitial Si generated during gate oxidation or implantation, so that OED or TED effects both in SiGeC and in nearby Si can be suppressed [10,14]. To use this principle for vertical MOSFET's, 20nm $Si_{0.976}Ge_{0.2}C_{0.004}$ layers grown at 625°C were sandwiched between the p^+ Si and the undoped spacers. Germane and methylsilane were used as the gas sources [15]. In addition to reducing the OED and TED effects, these layers also have the advantage that the boron diffusion coefficient in them is 80 times lower than in Si under the same N_2 annealing condition [16,17]. The SIMS profiles after all the high temperature processing is shown in Fig.5(a). The schematic structure is given in the inset. Note that in contrast to Fig. 4, the samples with SiGeC layers kept sharp boron profiles, so that it should be possible to reduce the channel length to under 50nm. In the sample of Fig. 5(a), the SiGeC was not doped, so that it was part of the channel. To remove the uncertainties about the effects of SiGeC and oxides grown on SiGeC on the channel carrier transport, we then heavily doped the SiGeC layers. This insured the channel region exists entirely in Si, and still allowed the device to benefit from the reduction of

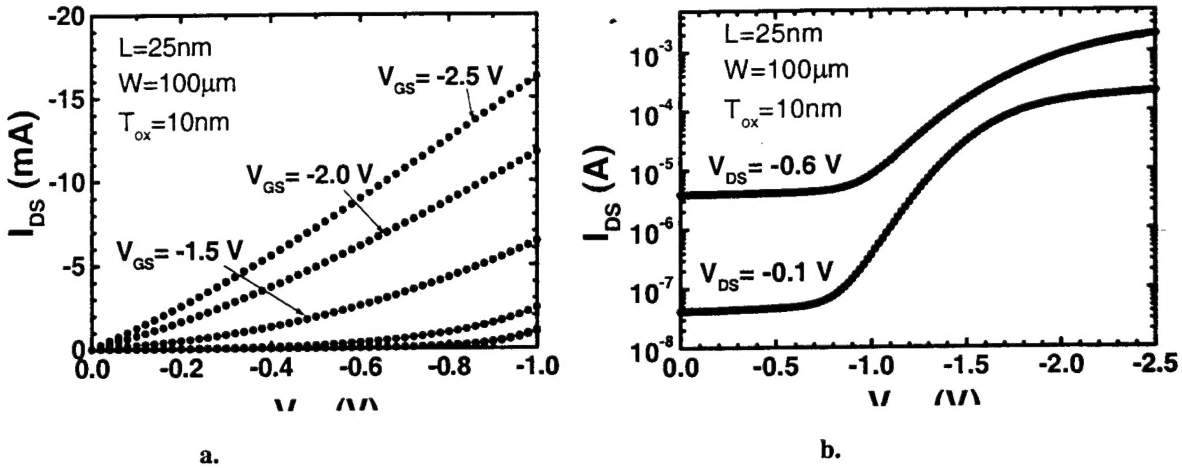
boron diffusion in the SiGeC region and nearby. Fig. 5(b) shows the SIMS profile in an actual L=25nm device sample after all the high temperature processing in which the SiGeC layers were doped.



a. b.

Figure 6: Output I-V (a) and subthreshold drain current vs. gate voltage (b) characteristic for L=70nm. Gate oxide was 6nm or 10nm measured on planar Si surface.

Well-behaved drain currents and subthreshold I-V curves for a transistor with channel length of 70nm are given in Fig. 6. L was measured by SIMS (as defined earlier) after all high temperature processing. A transconductance of 100mS/mm at V_{DS}= -1.1V has been achieved with a 6nm gate oxide on planar control wafer. Due to the high channel doping ($2.5x10^{18}cm^{-3}$), the subthreshold slopes are relatively large, 190mV/dec. Longer channel length devices (L=0.1μm) with lower doping ($0.9x10^{18}cm^{-3}$) and the same gate oxide thickness had better slopes (88mV/dec). To further scale the device, we also fabricated vertical p-channel MOSFET's with a 25nm channel length. These devices suffered from the onset of punch-through, but the gate still can control the drain current in the linear region (Fig. 7). Note the strained SiGeC has a bandgap 0.15eV lower than Si, with most of the offset in the valence band [18]. It has been predicted that narrower bandgap in source region would help reduce the floating body effects,[19] but their effect in present p-channel devices (low avalanche coefficient vs. n-channel) and low drain voltage is uncertain. Carriers crossing the heavily-doped SiGeC/Si interface may suffer from series resistance. The total series resistance in our device is 25Ω for W=200μm. It is not certain if it is due to the Si/SiGe interface or spreading and contact resistance. Improvements of the subthreshold and punch-through behavior will be expected using an ultra-thin pillar to fully deplete an intrinsic channel region by surrounding gates.



a. b.

Figure 7: Output I-V (a) and subthreshold drain current vs. gate voltage (b) for devices with L=25nm. Gate oxide was 10nm measured on planar Si surface.

Summary

Rapid thermal chemical vapor depositon (RTCVD) can be used to grow high quality $Si_{1-x-y}Ge_xC_y$ alloy layers. These layers are effective at reducing the oxidation enhanced diffusion of dopants by getting silicon interstitials not only in the $Si_{1-x-y}Ge_xC_y$ layers themselves, but also in nearby silicon layers. Vertical MOSFET's are an attractive option for the scaling of FET structures, by taking advantage of the ability of CVD to finely control layer thicknesses. By introducing SiGeC diffusion barrier layers, for the first time boron dopant diffusion from source and drain into the channel region can be suppressed during the gate oxidation of vertical p-channel MOSFET's. Devices with a channel length down to 25nm have been fabricated vs. a previous state of art of 130nm. Still better performance can be expected by using a surrounding gate structure with ultra-thin pillar.

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Technology Transition/Students Using the Equipment in this Program

Three Ph.D. students benefited directly rom the equipment supported by this program:

1. Ms. Min Yang:
   Thesis Title:Sub-100-nm Vertical MOSFET's with SiGeC Source/Drains
   Date of Graduation: June, 2000
   Current Employment: IBM Microelectronics, Fishkill, NY

2. Mr. Chialin Chang:
   Thesis Title: Properties and Applications of Crystalline SiGeC Alloys
   Date of Graduation: January, 1999
   Current Employment: Motorola, Phoenix, AZ

3. Dr. Louis Lanzerotti
   Thesis Title: Carbon in SiGe Heterojunction Bipolar Transistors
   Date of Graduation: January, 1999
   Current Employment: IBM Microelectronics, Burlington, VT

4. Mr. Malcolm Carroll
   Thesis Title: Fundamental Diffusion Effects in SiGeC and SiC alloys
   Date of Graduation: June 2001
   Current Employment: Agere Systems, Murray Hill, NJ

Ms. Yang, whose thesis was directly on the vertical MOSFET's discussed in this report, is now working at IBM Microelectronics on vertical MOSFET's for commercial product development using the expertise on these structures developed during her Ph.D.work at Princeton.

Publications Resulting from Equipment on this grant

1. C.C. Chang and J.C. Sturm, "Effect of carbon on the valence band offset of compressively-strained $Si_{1-x-y}Ge_xC_y$/ (100) Si heterojunctions," Appl. Phys. Lett. **(70)**, 1557-1559 (1997).

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